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1. A method of transmitting data traffic having a predetermined minimum transmittable element such as any one of a slot and a bit and being received from a number of prioritised sources comprising the steps of:

(a) setting the highest priority source with data traffic waiting for transmission as current transmission source;

(b) transmitting the data traffic from the current transmission source until completion whilst monitoring the sources for waiting traffic, wherein if traffic is detected from a source with a higher priority than the current transmission source going to step (d);

(c) upon completion, going to step (a); and,

(d) completing transmission of the current minimum transmittable element and going to step (a).

2. A method according to claim 1, in which step (b) comprises the further steps of adapting the data traffic before transmission to include, where not already present, one or more reassembly indicators for use in reassembling the data traffic upon receipt.

3. (Amended) A method according to claim 1[or 2], in which the minimum transmittable element for traffic of asynchronous and bit-synchronous protocols is a bit.

4. (Amended) A method according to claim 1[or 2], in which the minimum transmittable element for traffic of slot-synchronous protocols is a slot.

5. A method of reassembling a number of traffic streams interleaved within a data stream into a respective output queue for each traffic stream comprising the steps of:

(a) clearing the output queues and selecting a first output queue for receiving the data stream;

(b) passing the data stream to the selected output queue whilst monitoring the data stream, going to step (c) upon detection of a start indicator and going to step (d) if the end of a traffic stream is determined;

(c) selecting a further output queue to receive the data stream and going to step (b);

(d) if the memory stack contains one or more identifiers of output queues, retrieving the top identifier from the queue, selecting the output queue corresponding to the identifier to receive the data stream and going to step (b), going to step (a) otherwise.

6. A switch comprising a number of memory devices defining queues (1-4) for receiving traffic to be switched, each queue having an associated predetermined priority classification, and a processor for controlling the transmission of traffic from the queues (1-4) to an output (5,6), the processor being configured to transmit traffic from the higher priority classified queues before traffic from lower priority classified queues, the traffic having a predetermined minimum transmittable element such as any one of a slot and a bit, wherein the processor is configured to monitor the queues (1-4) to determine whether traffic has arrived at a queue having a higher priority classification than the queue from which traffic is currently being transmitted, the processor being responsive to suspend the current transmission after transmission of the current minimum transmittable element if traffic has arrived at a higher priority classified queue and thereafter transmit traffic from that queue, and subsequently resume the suspended transmission.

7. A switch according to claim 6, in which the processor is configured to adapt traffic received from the queues (1-4) to include one or more reassembly indicators, where not already present.

8. A switch according to claim 7, in which the reassembly indicators comprise different start (7) and end (9) indicators for each cell or packet in the traffic.

9. A switch according to claim 7, in which the reassembly indicators comprise start (7) and length indicators for each cell or packet in the traffic.

10. (Amended) A switch according to claim 7,[8 or 9,] in which the reassembly indicators include the queue's priority classification.

11. A switch according to claim 9, in which the processor is configured to adapt each packet or cell in the traffic received from the queues to include an indication of the queue's priority classification.

12. (Amended) A switch according to [any of claims 6 to 11]claim 6, wherein the processor is configured to store predetermined details of interrupted traffic transmissions and their respective queues in one of the memory devices and to retrieve the details for use in resuming the interrupted transmission once the interrupting transmission is completed.

13. (Amended) A switch according to [any of claims 6 to 12]claim 6, further comprising a number of outputs, wherein the processor is configured to transmit traffic to an appropriate output in dependence on the traffic's destination address.

14. (Amended) A switch according to [any of claims 6 to 13]claim 6, in which the minimum transmittable element for traffic of asynchronous and bit-synchronous protocols is a bit.

15. A switch according to any of claims 6 to 13, in which the minimum transmittable element for traffic of slot-synchronous protocols is a slot.

16. (Amended) A switch according to [any of claims 6 to 13]claim 6, in which the minimum transmittable element for traffic of slot-synchronous protocols is a slot.

17. A switch according to claim 16, in which the processor (20) is configured to monitor traffic, passing it to an output queue (30-60) until it detects a start indicator within the data stream, wherein the processor is configured to pass subsequent traffic to a further output queue until the end of an interleaved portion of traffic is determined, thereafter the processor is configured to pass subsequent traffic to the prior output queue, or until a further start indicator is detected within the data stream, wherein the processor is configured to pass subsequent traffic to a further output queue.

18. A switch according to claim 17, in which the end of an interleaved portion of traffic is determined in dependence on a portion length indicator within the interleaved portion of traffic.

19. A switch according to claim 17, in which the end of an interleaved portion of traffic is determined from end indicator within the data stream.

20. A switch according to claim 17, in which each interleaved portion of traffic includes a priority indicator, wherein the end of an interleaved portion of traffic is determined from a drop in level of the priority indicator.

21. (Amended) A switch according to claim 17[or 20], in which each interleaved portion of traffic includes a priority indicator, wherein a start indicator comprises a rise in the level of the priority indicator.

22. (Amended) A switch according to [any of claims 17 to 21]claim 17, in which the processor (20) is configured to operate as state machine.

23. (Amended) A telecommunications network comprising a switch as claimed of [claims 6 to 22]claim 6.

24. (Amended) A computer program product comprising a number of computer executable instructions for executing the steps of [any of claims 1 to 5]claim 1.